

## CLAIMS

What is claimed is:



1                   --A controller chip comprising:  
2                   an engine for managing a memory and including an interface; and  
3                   a storage element coupled to the engine, the storage element being accessible by  
4                   a central processing unit (CPU), wherein the engine receives commands from the CPU via the  
5                   interface, manages the storage element and writes the commands into the memory.

- 1                   2.       The controller chip of claim 1 wherein the storage element comprises a first in  
2                   first out (FIFO) buffer.
- 1                   3.       The controller chip of claim 2 in which the FIFO buffer comprises a circular  
2                   FIFO buffer.
- 1                   4.       The controller chip of claim 2 in which the FIFO buffer comprises a double  
2                   buffer.
- 1                   5.       The controller chip of claim 2 in which the FIFO buffer comprises a triple  
2                   buffer.
- 1                   6.       The controller chip of claim 3 wherein the effective size of the FIFO buffer as

2 viewed by the CPU can be as large as the memory.

1 7. The controller chip of claim 2 which includes a checking mechanism for  
2 determining if the FIFO buffer needs to be emptied without utilizing the CPU.

3 8. The controller chip of claim 7 wherein the checking mechanism comprises:  
4 means for calculating the time required to fill the FIFO buffer;  
5 means for determining if the used memory of the FIFO buffer is below a  
predetermined amount based upon the time required to fill the FIFO buffer; and  
means for preventing the FIFO buffer from filling if the used memory in the  
FIFO buffer is over the predetermined amount.

6 9. The controller chip of claim 1 wherein the controller chip comprises a graphics  
controller chip.

10. The controller chip of claim 9 wherein the engine comprises a graphics engine.

1 1.1. A system for providing a command stream in a computer system comprising:  
2 a central processing unit (CPU);  
3 a controller coupled to the CPU and including an interface;  
4 a memory coupled to the controller, the memory being managed by the  
5 controller; and

6 a storage element coupled to the controller, the storage element being accessible  
7 by the CPU, wherein the controller receives commands from the CPU via the interface,  
8 manages the storage element and writes the commands into the memory.

1 12. The system of claim 11 wherein the storage element comprises a first in first  
2 out (FIFO) buffer.

1 13. The system of claim 12 in which the FIFO buffer comprises a circular FIFO  
2 buffer.

1 14. The system of claim 12 in which the FIFO buffer comprises a double buffer.

1 15. The system of claim 12 in which the FIFO buffer comprises a triple buffer.

1 16. The system of claim 12 in which the controller comprises a graphics controller.

1 17. The system of claim 12 wherein the effective size of the FIFO buffer can be as  
2 large as the memory.

1 18. The system of claim 12 which includes a checking mechanism for determining  
2 if the FIFO buffer needs to be emptied without utilizing the CPU.

1 19. The system of claim 18 wherein the checking mechanism comprises:  
2 means for calculating the time required to fill the FIFO buffer;  
3 means for determining if the FIFO buffer is below a predetermined amount  
4 based upon the time required to fill the buffer; and  
5 means for preventing the FIFO buffer from filling if the FIFO buffer is above  
6 the predetermined amount.

1 20. A method for providing a command stream in a computer system, the computer  
2 system including a central processing unit (CPU), a controller coupled to the CPU, a memory  
3 coupled to the controller, the memory being managed by the controller; the method comprising  
4 the steps of:  
5 (a) providing a storage element within the controller; and  
6 (b) allowing the storage element to be accessible by the CPU via an interface in the  
7 graphics controller.

1 21. The method of claim 20 wherein the storage element comprises a FIFO buffer.

1 22. The method of claim 21 in which the FIFO buffer comprises a circular FIFO  
2 buffer.

1 23. The method of claim 21 in which the FIFO buffer comprises a double buffer.

1 24. The method of claim 21 in which the FIFO buffer comprises a triple buffer.

1 25. The method of claim 21 in which the memory comprises a graphics memory.  
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1 26. The method of claim 21 wherein the effective size of the FIFO buffer as viewed  
2 by the CPU can be as large as the memory.

1 27. The method of claim 21 which includes the step of (c) determining if the FIFO  
2 buffer needs to be emptied without utilizing the CPU.

1 28. The method of claim 27 wherein the determining step (c) further comprises:  
2 (c1) calculating the time required to fill the FIFO buffer;  
3 (c2) determining if the FIFO buffer is below a predetermined amount based  
4 upon the time required to fill the buffer; and  
5 (c3) preventing the FIFO buffer from filling if the FIFO buffer is above the  
6 predetermined amount.